What is claimed is:

1. A temperature sensing device comprising:
a temperature variant oscillator that generates a variable rate signal having a frequency that varies in response to a temperature of the device;
a temperature invariant oscillator that generates a fixed width signal indicating a sense cycle; and
a counter that generates an n-bit count value in response to the variable rate signal and the fixed rate signal, the n-bit count value indicating the temperature.

2. The device of claim 1 wherein the n-bit count value is 16 bits.

3. The device of claim 1 wherein the fixed rate signal enables the counter when a temperature sense period is desired and the variable rate signal clocks the counter.

4. The device of claim 1 wherein the counter is reset prior to each sense cycle.

5. The device of claim 1 wherein a warmer temperature is indicated by a larger count value and a colder temperature is indicated by a smaller count value.

6. The device of claim 1 wherein the device is embedded in a memory circuit.

7. The device of claim 6 wherein the memory circuit is a dynamic random access memory and the memory circuit refresh rate is changed in response to the temperature sensed by the device.

8. The device of claim 7 wherein the refresh rate is increased for warmer temperatures and decreased for colder temperatures.

9. A temperature sensing device comprising:

a temperature variant oscillator that generates a variable rate signal having a frequency that varies in response to a temperature of the device;

a temperature invariant oscillator that generates a fixed width signal indicating a sense cycle;

a counter that generates an n-bit count value in response to the variable rate signal and the fixed rate signal, the n-bit count value indicating the temperature; and

an oscillator read logic, coupled to the temperature invariant oscillator and the counter, for resetting the counter to a default status and triggering the temperature invariant oscillator to generate the fixed width signal.

10. The device of claim 9 wherein the default status is zero.

11. The device of claim 9 wherein the fixed width signal is a logically high signal and the variable rate signal comprises logically high pulses to clock the counter.

12. The device of claim 9 wherein the fixed width signal is generated at predetermined intervals in a range of 500 milliseconds to 1 second.

13. The device of claim 9 wherein the fixed width signal has a width measured in milliseconds.

14. A memory device comprising:

a memory array for storing data;

a memory controller that generates control signals, including refresh signals, to the memory array; and

a temperature sensing device, coupled to the memory controller, for sensing a temperature of the memory device, the temperature sensing device comprising:

a temperature variant oscillator that generates a variable rate signal having a frequency that varies in response to a temperature of the memory device;

a temperature invariant oscillator that generates a fixed width signal indicating a sense cycle; and

a counter that generates an n-bit count value in response to the variable rate signal and the fixed rate signal, the n-bit count value indicating the temperature of the memory device.

15. The memory device of claim 14 wherein the memory array is a dynamic memory array.

16. The memory device of claim 14 wherein a frequency of the refresh signals is increased as the temperature of the memory device increases and the frequency of the refresh signals is decreased as the temperature of the memory device decreases.

17. An electronic device comprising:

a microprocessor that generates control signals for the electronic device;

a memory device comprising:

a memory array for storing data;

a memory controller that generates control signals, including refresh signals, to the memory array; and

a temperature sensing device, coupled to the memory controller, for sensing a temperature of the memory device, the temperature sensing device comprising:

a temperature variant oscillator that generates a variable rate signal having a frequency that varies in response to a temperature of the memory device;

a temperature invariant oscillator that generates a fixed width signal indicating a sense cycle; and

a counter that generates an n-bit count value in response to the variable rate signal and the fixed rate signal, the n-bit count value indicating the temperature of the memory device.

18. The electronic device of claim 17 and further including a battery that powers the electronic device such that the temperature sensing device senses the temperature of the battery.

19. A method for sensing a temperature of an integrated circuit, the method comprising:

generating a clocking signal having a rate that varies with the temperature of the integrated circuit;

generating an enable signal to enable a counter circuit; and

generating a count value in response to the clocking signal and the enable signal, the count value indicating the temperature of the integrated circuit.

20. The method of claim 19 wherein the count value is higher for warmer temperatures and lower for colder temperatures.

21. The method of claim 19 and further including resetting the count value to a default value prior to enabling the counter circuit.

22. The method of claim 21 wherein the default value is zero.

23. A method for reading a temperature indication from a temperature sensing circuit embedded in a memory circuit, the method comprising:

performing at least one asynchronous read cycle to a predetermined memory address of the memory circuit;

performing at least one asynchronous write cycle comprising a data pattern that indicates an internal register of the temperature sensing circuit;

reading the temperature indication off of a data bus in the memory circuit.

24. The method of claim 23 wherein the predetermined memory address a highest address in a memory address range of the memory circuit.

25. The method of claim 23 wherein the data pattern is 02H and indicates the internal register assigned to the temperature sensing device.

26. The method of claim 23 wherein the at least one asynchronous read cycle and the at least one asynchronous write cycle are each performed twice.

27. The method of claim 23 and further including:

increasing a refresh rate of the memory circuit in response to the temperature indication indicating a warmer temperature; and

decreasing the refresh rate of the memory circuit in response to the temperature indication indicating a colder temperature.

28. A method for measuring a temperature of a battery-powered electronic device while charging the battery, the electronic device having a memory circuit, the method comprising:

measuring an ambient temperature with a temperature sensing device embedded in the memory circuit;

initiating the charging process;

measuring the temperature of the battery with the temperature sensing device;

correcting the measured battery temperature in response to the ambient temperature to produce a corrected battery temperature; and

when the corrected battery temperature indicates a temperature acceleration that is greater than a predetermined threshold, reducing a charging current to the battery.

29. The method of claim 28 wherein measuring the ambient temperature and measuring the temperature of the battery comprise:

performing at least one asynchronous read cycle to a predetermined memory address of the memory circuit;

performing at least one asynchronous write cycle comprising a data pattern that indicates an internal register of the temperature sensing circuit;

reading the temperature indication off of a data bus in the memory circuit.